2.6 A 60μW 60 nV/√Hz Readout Front-End for Portable Biopotential Acquisition Systems

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Electroencephalogram (EEG), Electrocardiogram (ECG), and Electromyogram (EMG) waves are μV range signals that are correlated by large amount of common-mode (CM) interference. Moreover, there is offset of the biopotential electrodes. To achieve signal extraction under these circumstances, a front-end is needed with high CMRR, low-noise, HPF characteristics and configurability for different biopotentials. Furthermore, very low-power consumption is necessary to achieve long-term power autonomy. The aim is not only to increase the patient's autonomy and quality of life, but also to extend the device applications to sports, entertainment, comfort monitoring, etc.

Chopping is a frequently used technique for implementing high CMRR and low-noise front-ends [1]. However, chopping amplifiers are inherently DC coupled devices. Figure 2.6.1 shows the concept of the proposed AC coupled chopped instrumentation amplifier (IA). It uses a current feedback IA to achieve lower power dissipation than its resistive counterparts [2]. A LPF with a cut-off frequency, f_p, senses the output voltage of the IA, and cancels the current supplied by the IA. If the transconductance, g_m, of the LPF is much larger than $1/R_1$ and $1/R_2$, this topology implements a HPF (1).

$$V_{out}/V_{in} = (R_2/R_1)\cdot(s+2\pi f_p)/(s+2\pi g_m R_2 f_p) \quad (1)$$

Figure 2.6.1 also shows the implementation of the AC coupled chopped IA with the simplified schematic of the proposed current feedback IA, which consists of only 4 parallel branches for low power dissipation. If the total resistance, R_{out}, at nodes A and B can be increased, the first two terms in the denominator of (2) vanish and the ratio of two resistors defines the gain of the IA. However, usage of conventional cascode transistors at the input, as in a telescopic opamp, results in a reduction of the output voltage swing as the input voltage swing is increased. To avoid this, an active cascode input stage is implemented as shown in Fig. 2.6.2. This active stage copies the voltage at the source of M_1 to the drain of M_1 with a DC offset defined by the gate-to-source voltage differences of M_3 and M_4, defining the drain-to-source voltage (V_{ds}) of M_1. Hence, this input stage reduces the dependency between input and output voltage swings compared to a conventional cascode stage. Additionally, the proposed input stage prevents the reduction of the CMRR under electrode offset [3], due to the immunity of the V_{ds} of the input transistors from the input voltage level. It is important to realize that chopping cannot prevent CMRR reduction due to the electrode offset, since the input chopper also modulates the electrode offset. Similarly, the LPF, filtering the electrode offset, prevents the reduction of the CMRR under electrode offset by preserving the current symmetry under the chopped electrode offset. Figure 2.6.2 shows the CMRR measurement of the IA and the change of the CMRR with changing DC electrode offset. CMRR of the chopped IA is better than 120dB up to 1kHz and better than 110dB, measured at 100Hz, with 50mV DC electrode offset.

$$\frac{V_{out}}{V_{in}} = 1\Big/\left[\left(1+\frac{1}{gm_{2,3}R_2}\right)\frac{1}{gm_{1,4}R_{out}}+\frac{R_1}{R_{out}}\left(1+\frac{1}{gm_{2,3}R_2}\right)+\frac{R_1}{R_2}\right]=\frac{R_2}{R_1} \quad (2)$$

Figure 2.6.3 shows the schematic of the biopotential front-end. It includes the AC coupled chopped IA clocked at 4kHz, a SC spike filter (SF) stage, a constant gain stage [4], and a VGA. A common problem of chopper amplifiers is the spikes at the output [1]. These spikes appear at the even harmonics of the chopping frequency and can reduce the CMRR of the IA due to CM modulated charge injection [5]. Moreover, high frequency spike components can fold over into the base band, if a sampling ADC, like a SAR, is used after the front-end. Therefore, we propose a simple and low-power (800nA) SF technique, Fig. 2.6.3, where the output spikes can be reduced more than 20dB by opening the switches S_1 and S_2 during the presence of a spike.

A configurable front-end should have adjustable gain for different biopotential signals. Conventional low-power implementations use SC amplifiers for implementing the VGA resulting in fold over of noise and signals above the Nyquist frequency [1]. Therefore, we propose a CT VGA block, Fig. 2.6.3, where gain is defined by the ratio of the two capacitors. Gain is adjusted by changing the effective value of the total capacitance between nodes in- and ground via the gain select switches. Furthermore, the VGA exhibits LPF characteristics, further filtering the residual high frequency signals. Figure 2.6.4 shows the measured gain-bandwidth of the front-end with changing VGA settings. The external capacitor, C_1, of Fig. 2.6.1, and the BW select switches control low and high cut-off frequencies, respectively.

Figure 2.6.5 shows the measured output noise PSD of the complete front-end at a gain of 800 with a BW of 0.3Hz-350Hz. Total integrated input referred noise of $1.12\mu V_{rms}$ is measured with chopping and SF. The residual flicker noise has negligible contribution on the total noise and is due to the stages following the IA. Figure 2.6.5 shows that SF does not affect the noise, due to the small duty cycle of the hold time and sampling frequency of two times the chopping frequency [1]. Assuming that all the measured noise is generated by the IA, the IA achieves a noise-efficiency factor (NEF) [6] of 7.8, while dissipating 11.1μA from 3V. Figure 2.6.5 shows the power-noise performance comparison of the implemented IA. The only IA [4] achieving a better NEF not only has very low CMRR, which makes it unsuited for extracting clean biopotential signals, but also features a fixed low cut-off frequency, which prevents its use for EMG (10–20Hz) applications.

Figure 2.6.6 shows the extracted biopotential signals from the readout front-end, EEG, ECG and EMG, and summarizes the measured results from the biopotential readout front-end. The front-end has been fabricated in a 0.5μm CMOS process through AMIS and the core area measures less than 2mm², shown in Fig. 2.6.7, and is capable of operating more than 3 years from 2 conventional AA batteries. Therefore, it is very suitable for autonomous applications.

References:

[1] C. C. Enz and G. C. Temes, "Circuit Techniques for Reducing the Effects of Opamp Imperfections," *Proc. of the IEEE,* vol. 84, no. 11, pp. 1584-1614, Nov., 1996.
[2] R. Martins et. al., "A CMOS IC for Portable EEG Acquisition Systems," *IEEE Trans. on Inst. and Meas.*, vol. 47, no. 5, pp. 1191-1196, Oct., 1998.
[3] R. F. Yazicioglu, P. Merken, and C. Van Hoof, "Integrated Low-Power 24-channel EEG Front-End," *IEE Electronics Letters*, vol. 41, no. 8, pp. 457-458, Apr., 2005.
[4] R. R. Harrison and C. Charles, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications," *IEEE J. Solid State Circuits*, vol. 38, no. 6, pp. 958-965, June, 2003.
[5] C. Menolfi and Q. Huang, "A Fully Integrated, Untrimmed CMOS Instrumentation Amplifier with Submicrovolt Offset," *IEEE J. Solid State Circuits*, vol. 34, no. 3, pp. 415-420, Mar., 1999.
[6] M. S. J. Steyaert et. al., "A Micropower Low-Noise Monolithic Instrumentation Amplifier for Medical Purposes," *IEEE J. Solid State Circuits,* vol. 22, no. 12, pp. 1163-1168, Dec., 1987.

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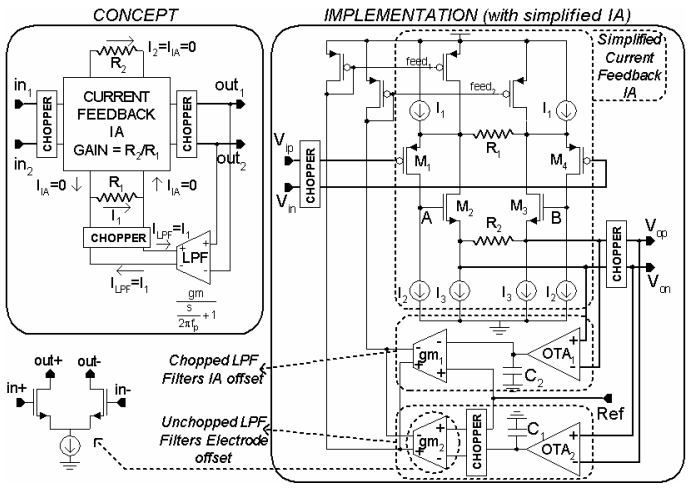


Figure 2.6.1: Concept and implementation of the AC coupled chopped IA.

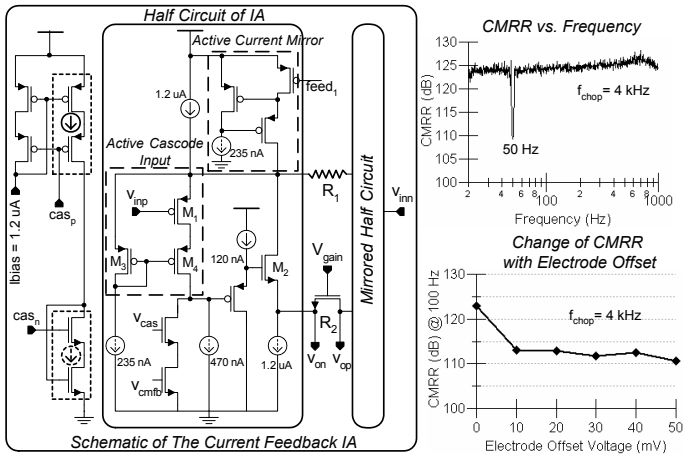


Figure 2.6.2: Complete IA schematic and CMRR measurement results.

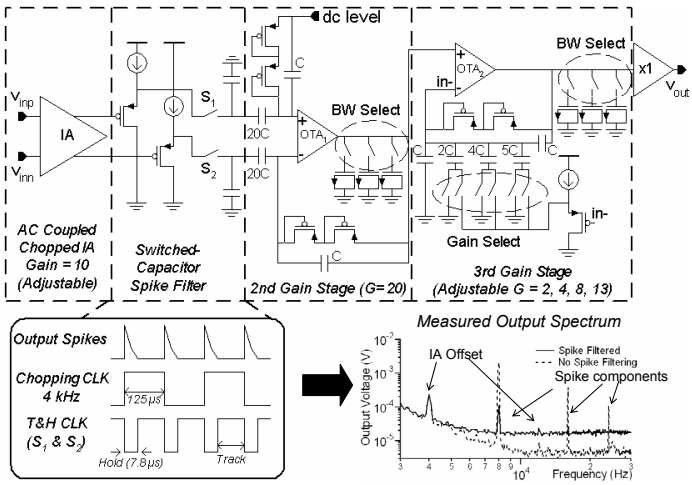


Figure 2.6.3: Readout front-end schematic, and operation and test result of SF.

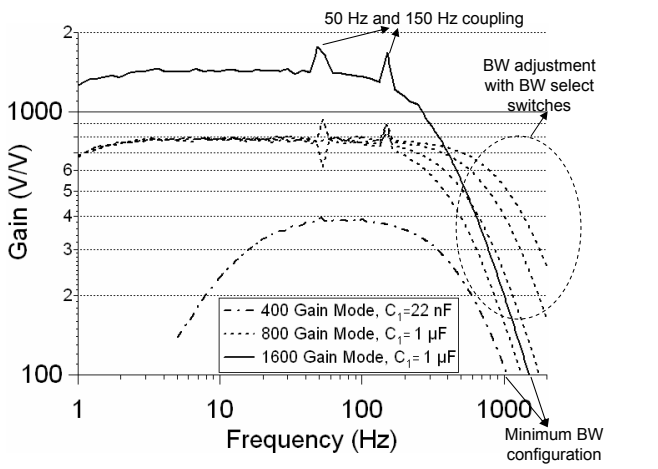


Figure 2.6.4: Gain-bandwidth measurement of the front-end with changing gain and bandwidth settings.

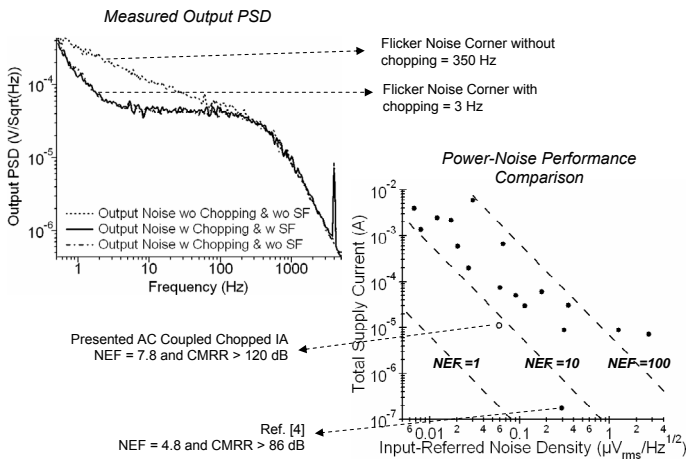
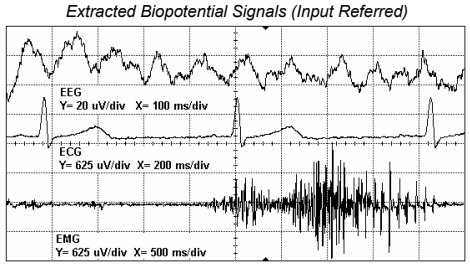


Figure 2.6.5: Measured output PSD of front-end and power-noise performance comparison of IA.



Current Consumption of Channel Blocks

Building Blocks of Front-End	*Current Cons.*
Chopped IA	11.1 µA
Spike Filter	800 nA
Second Gain Stage	1.4 µA
Third Gain Stage	750 nA
Channel Buffer	2.4 µA
Bias Buffer Opamps	2*0.6 µA
Bias Circuit	2.4 µA
Total Current Consump.	**20 µA**
Total Power Dissipation	**60 µW**

Measured Characteristics of the Front-End

Voltage Supply	3 V
Current Consumption	20 µA
Electronic Gain Selection	390, 800, 1450, 2500
Continuous Gain Adjustment	via R_2
Equivalent Input Referred Noise	60 $nV/\sqrt{Hz}$
CMRR (0 mv Electrode Offset)	>120 dB
CMRR (50 mV Electrode Offset)	> 110 dB
Low cut-off frequency	Adjustable via external capacitance
High cut-off frequency	Electronically selectable

Figure 2.6.6: Extracted biopotential signals from the readout front-end, and the summary of the results.

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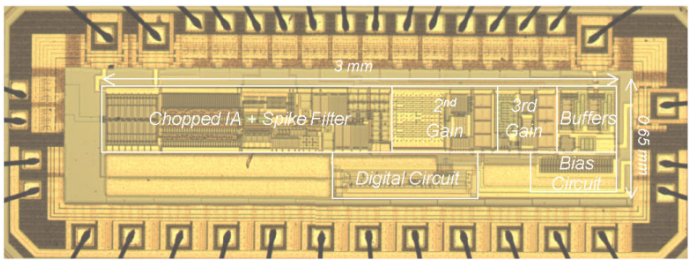

Figure 2.6.7: Chip micrograph of the biopotential readout front-end.

